Chip Package System

CIMPACA - Sophia Antipolis - February 2018

Jerome.Toublanc@ansys.com
ANSYS is About Simulations

FOCUSED
This is all we do.
Leading product technologies in all physics areas
Largest development team focused on simulation

CAPABLE
2,700+ employees
75 locations
40 countries

PROVEN
Recognized as one of the world’s MOST INNOVATIVE AND FASTEST-GROWING COMPANIES*

TRUSTED
96 of the top 100 FORTUNE 500 industrials
ISO 9001 certified

INDEPENDENT
Long-term financial stability
CAD agnostic

LARGEST
3x The size of our nearest competitor

*BusinessWeek, FORTUNE
ANSYS Solution Offerings

Leading Disciplines

Fluids  Structures  Electromagnetics  Thermal  Power Integrity  Systems  Embedded Software

Global Reach

PEOPLE

1,375+  650+  800+  2,000+

CUSTOMERS

45,000+ GLOBALLY

Industry Presence

ANSYS Solution Offerings

Deepest & Broadest portfolio
Electronic & SemiConductor Business Units

Driving Chip-Package-System Convergence

End-to-End Chip-Package-System
Power, Noise, Thermal, EMI, Timing Platform
SemiConductors Business Unit

RedHawk References

Top 20 Semi

<table>
<thead>
<tr>
<th>Company</th>
<th>Headquarters</th>
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</thead>
<tbody>
<tr>
<td>Intel</td>
<td>U.S.</td>
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<tr>
<td>Samsung</td>
<td>South Korea</td>
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<tr>
<td>TSMC*</td>
<td>Taiwan</td>
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<tr>
<td>Qualcomm**</td>
<td>U.S.</td>
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<td>Micron + Elpida</td>
<td>U.S.</td>
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<tr>
<td>SK Hynix</td>
<td>South Korea</td>
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<tr>
<td>TI</td>
<td>U.S.</td>
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<tr>
<td>Toshiba</td>
<td>Japan</td>
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<td>Broadcom**</td>
<td>U.S.</td>
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<tr>
<td>ST</td>
<td>Europe</td>
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<tr>
<td>Renesas</td>
<td>Japan</td>
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<td>MediaTek + MStar**</td>
<td>Taiwan</td>
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<td>Infineon</td>
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<td>NXP</td>
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<td>AMD**</td>
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<td>Sony</td>
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<td>Avago + LSI**</td>
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<td>Freescale</td>
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<td>Nvidia**</td>
<td>U.S.</td>
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</table>

In the news

Networking
Clarifly Engages ANSYS Power Software To Develop 100- To 400-Gigabit Semiconductor Solutions

Automotive
NXP Semiconductors Leverages ANSYS Solutions To Develop Innovative Car Infotainment System

Mobile, Computing
ANSYS Power Noise And Reliability Solutions Adopted By Fujitsu For High-Performance Processor Designs

Consumer / IoT
Atmel Uses ANSYS Simulation Solutions To Power The Internet Of Things

Motivations

SoC Modeling
Mixed Analog-Digital
Power Integrity
ESD

SignOff
Chip Failure Debugging
Best-in-Class

SignOff
Foundry Certified

Reliability
Substrate Analysis
Chip-Package coAnalysis
Industry Standard

Mitigate Risks!
Power Integrity
- Are devices properly supplied to guaranty chip performances in every possible operational modes?

Power Reliability
- Does the Power Delivery Network fully support the Current Consumption and Distribution?

Thermal Integrity
- How Chip Power gets dissipated? How Self Heating impacts Chip Reliability?

ESD Reliability
- Are the instantiated ESD protections fully efficient?
SemiConductor Business Unit

What do we simulate?

It is about Switching Cells!

Switching Transistors
Dynamic SoC Simulation

It is about Switching Current!

Switching Power:

- **Average current** = \( f(f \text{req}, \text{charge, } V) = \frac{1}{2} C.V^2 \cdot \text{freq} \)
- **Peak current** = \( f(\text{slew, charge, transition, } V) \)

Clock Buffer:
- **CaseA**: Load C & Freq f
- **CaseB**: Load 2C & Freq \( \frac{1}{2}f \)

**Same Average, Different Dynamic Current!**
Dynamic SoC Simulation
It is about Switching Current!

Switching Power:

Average current = \( f(freq, \text{charge, V}) = \frac{1}{2} C.V^2.f\)req
Peak current = \( f(\text{slew, charge, transition, V}) \)

<table>
<thead>
<tr>
<th>Technology</th>
<th>Supply Value Volt</th>
<th>Gate Density #/mm²</th>
<th>Peak Current mA/gate</th>
<th>Loading Cap fF/gate</th>
<th>Peak Current A/mm²</th>
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<tbody>
<tr>
<td>1.2μm</td>
<td>5</td>
<td>8K</td>
<td>1.10</td>
<td>60</td>
<td>8.8</td>
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<tr>
<td>0.8μm</td>
<td>5</td>
<td>15K</td>
<td>0.90</td>
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<td>13.5</td>
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<td>5</td>
<td>28K</td>
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<td>5 - 3.3</td>
<td>50K</td>
<td>0.60</td>
<td>25</td>
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<tr>
<td>0.25μm</td>
<td>5 - 2.5</td>
<td>90K</td>
<td>0.40</td>
<td>20</td>
<td>36</td>
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<tr>
<td>0.18μm</td>
<td>3.3 - 2</td>
<td>160K</td>
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<td>0.12μm</td>
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<td>0.20</td>
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<td>90nm</td>
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<td>2000K</td>
<td>0.05</td>
<td>3</td>
<td>100</td>
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</table>

It is about SSN!
Simultaneous Switching Noise

28nm -> ~4000K/mm²
20nm -> ~7000K/mm²
FinFet 14nm -> ~9000K/mm²
FinFet 7nm -> ~17M/mm² @ 0.5V

Peak Current & Technology
Dynamic SoC Simulation

It is about Local Voltage Drop

That’s where Decap Cells can help!
Dynamic SoC Simulation

It is about Global Voltage Drop

That’s where Scan Chain Optimization can help!
Dynamic SoC Simulation
Voltage Drop Impact on Project

Logic Failure?
✓ Validate Voltage Threshold

Timing Failure?
✓ Validate Impact on Timing

Clock Failure?
✓ Validate Impact on Clock

ΔV_{min} ok?

ΔV@t1 ok?

Resonance freq

ΔV@t1

ΔV_{min}

clk

FF

vdd

gnd

vdd

clk

gnd

Signal

Ideal

True

Resonance freq

Clock

Ideal

jitter
RedHawk

Power, Noise & Reliability Platform for SoC

1. Power/Ground Network Extraction
2. Power Analysis
3. Power/Ground Network Simulation
4. Export of Simulated SoC Models
RedHawk Use Case

Explore the Simulation

Activity Analysis
✓ Over time
✓ Switching Noise
✓ Peak Activity
✓ Local vs. Global

Current vs. time
✓ Per layer
✓ Per pin
✓ Per Cell
✓ Per Transistor

Voltage vs. Time
✓ Per layer
✓ Per pin
✓ Per cell
✓ Per transistor

Drop over Time / Current over Time / Activity over Time
RedHawk Use Case

Chip Power Modeling (CPM)

Memories
Analog
Digital
Topologies/PDN

200MHz
120MHz
50MHz
31.25MHz

Frequencies

Activity

Package

Spice Model of Power/Ground SoC pins

Intrinsic PDN Parasitics

Current Signature

Intrinsic PDN
Parasitics

Parasitics

Current Signature

RedHawk Use Case

Chip Power Modeling (CPM)

Spice Model of Power/Ground SoC pins

Intrinsic PDN Parasitics

Current Signature

RedHawk Use Case

Chip Power Modeling (CPM)

Spice Model of Power/Ground SoC pins

Intrinsic PDN Parasitics

Current Signature

RedHawk Use Case

Chip Power Modeling (CPM)

Spice Model of Power/Ground SoC pins

Intrinsic PDN Parasitics

Current Signature
Chip-Package-System Simulations

Power, Thermal, Reliability, EMI and SI

Thermal
SIwave - IcePack

Signal
SIwave - AEDT

ESD
AEDT - HFSS

Make PCB Simulations « Chip-Aware »
ANSYS Chip-Package-System ecosystem

ASIC (Application Specific Integrated Circuit)

Company A

CMA – HFSS – Slwave - Icepak
«Chip Aware» System Simulations

PowerArtist
RTL Power Analysis

RTL Designer

ASIC

ANSYS-CPS eco-system

Chip Models

RTL Models

RedHawk
SoC Power Integrity & Reliability

SoC Designer

IP Company

Totem
Analogue IP Integrity & Reliability

Analogue Designer

Analog-Digital Mixed-Analysis

ASIC Company

Slwave
Package Extraction and Analysis

Package Designer

Package Company

PCB Designer
Thank you

Merci